Compact +30 V / ±15 V 256-Position Digital Potentiometer

Preliminary Technical Information

AD5290

FEATURES

256-position
10 kΩ, 50 kΩ, 100 kΩ
+4.5 V to +30 V single-supply operation
±4.5 V to ±15 V dual-supply operation
3-wire SPI-compatible serial interface
Low-temperature coefficient 35ppm/°C typical
THD 0.006% typical
Midscale preset
Compact MSOP-10 package
Automotive temperature range -40°C to +125°C
***i*CMOS™[1] process technology**

APPLICATIONS

High-voltage DAC
Programmable power supply
Programmable gain and offset adjustment
Programmable filters, delays
Actuator control
Audio volume control
Mechanical potentiometer replacement

FUNCTIONAL BLOCK DIAGRAM

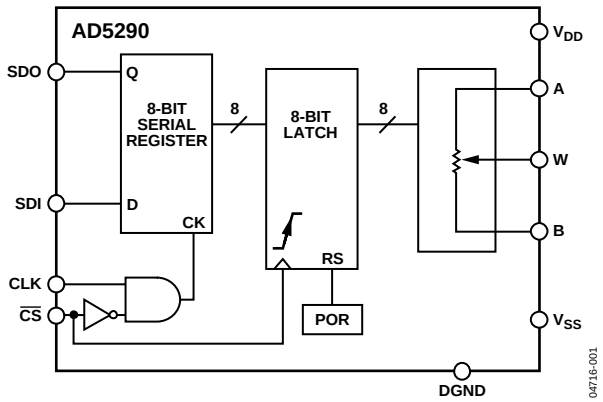

Figure 1.

GENERAL DESCRIPTION

The AD5290 is one of the few high voltage, high performance, and compact digital potentiometers[2] in the market at present. This device can be used as a programmable resistor or resistor divider. The AD5290 performs the same electronic adjustment function as mechanical potentiometers, variable resistors, and trimmers, with enhanced resolution, solid-state reliability, and superior temperature stability.

With digital rather than manual control, AD5290 provides layout flexibility and allows close-loop dynamic controllability.

The AD5290 is available in MSOP-10 package in 10 kΩ, 50 kΩ, and 100 kΩ options. All parts are guaranteed to operate over the –40°C to +125°C extended automotive temperature range.

[1] *i*CMOS™ Process Technology. For analog systems designers who need high performance ICs at higher-voltage levels, *i*CMOS is a technology platform that enables the development of analog ICs capable of 30 V and operating at ±15 V supplies while allowing dramatic reductions in power consumption and package size, and increased AC and DC performance.
[2] The terms digital potentiometer and RDAC are used interchangeably.

Rev. PrF

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REVISION HISTORY

Revision 0: Initial Version

AD5290–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—10 kΩ VERSION

V_{DD}/V_{SS} = ±15 V ± 10%, V_A = $+V_{DD}$, V_B = V_{SS}/0 V, −40°C < T_A < +125°C, unless otherwise noted.
Table 1.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS RHEOSTAT MODE						
Resistor Differential NL[2]	R-DNL	R_{WB}, V_A = NC, V_{DD}/V_{SS} = ±15 V	−1	±0.5	+1	LSB
Resistor Nonlinearity[2]	R-INL	R_{WB}, V_A = NC, V_{DD}/V_{SS} = ±15 V	−1	±0.5	+1	LSB
Nominal Resistor Tolerance	ΔR_{AB}	T_A = +25°C	−30		+30	%
Resistance Temperature Coefficient[3]	$(\Delta R_{AB}/R_{AB})/\Delta T*10^6$	V_{AB} = V_{DD}, wiper = no connect		35		ppm/°C
Wiper Resistance	R_W	V_{DD}/V_{SS} = ±15 V		120	200	Ω
		V_{DD}/V_{SS} = ±5 V		260		Ω
DC CHARACTERISTICS POTENTIOMETER DIVIDER MODE						
Integral Nonlinearity[4]	INL	V_{DD}/V_{SS} = ±15 V	−1	±0.5	+1	LSB
Differential Nonlinearity[4]	DNL	V_{DD}/V_{SS} = ±15 V	−1	±0.5	+1	LSB
Voltage Divider Temperature Coefficient	$(\Delta V_W/V_W)/\Delta T*10^6$	Code = 0x80		5		ppm/°C
Full-Scale Error	V_{WFSE}	Code = 0xFF, V_{DD}/V_{SS} = ±15 V	−3	−1.5	0	LSB
Zero-Scale Error	V_{WZSE}	Code = 0x00, V_{DD}/V_{SS} = ±15 V	0	+1.5	+3	LSB
RESISTOR TERMINALS						
Voltage Range[5]	$V_{A, B, W}$		V_{SS}		V_{DD}	V
Capacitance[6] A, B	$C_{A, B}$	f = 1 MHz, measured to GND, code = 0x80		45		pF
Capacitance[6]	C_W	f = 1 MHz, measured to GND, code = 0x80		60		pF
Common-Mode Leakage	I_{CM}	V_A = V_B = V_W		1		nA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High ($\overline{CS}$, CLK, SDI)	V_{IH}	V_{DD} = 5 V or 15 V	2.4			V
Input Logic Low ($\overline{CS}$, CLK, SDI)	V_{IL}	V_{DD} = 5 V or 15 V			0.8	V
Output Logic High (SDO)	V_{OH}	$R_{Pull-up}$ = 2.2 kΩ to 5 V	4.9			V
Output Logic Low (SDO)	V_{OL}	I_{OL} = 1.6 mA, V_{LOGIC} = 5 V, V_{DD} = 15 V			0.4	V
Input Current	I_{IL}	V_{IN} = 0 V or 5 V			±1	µA
Input Capacitance[6]	C_{IL}			5		pF
POWER SUPPLIES						
Power Supply Range	V_{DD}/V_{SS}	Dual-supply range	±4.5		±16.5	V
Power Supply Range	V_{DD}	Single-supply range, V_{SS} = 0	4.5		33	V
Positive Supply Current	I_{DD}	V_{IH} = +5 V or V_{IL} = 0 V, V_{DD}/V_{SS} = ±15 V			2	mA
		V_{IH} = +5 V or V_{IL} = 0 V, V_{DD}/V_{SS} = ±5 V		12	25	µA
Negative Supply Current	I_{SS}	V_{IH} = +5 V or V_{IL} = 0 V, V_{DD}/V_{SS} = ±15 V			−0.1	mA
		V_{IH} = +5 V or V_{IL} = 0 V, V_{DD}/V_{SS} = ±5 V			−0.1	mA
Power Dissipation[7]	P_{DISS}	V_{IH} = +5 V or V_{IL} = 0 V, V_{DD}/V_{SS} = ±15 V			31.5	mW
Power Supply Rejection Ratio	PSRR	$\Delta V_{DD}/\Delta V_{SS}$ = ±15 V ±10%	−0.2	±0.05	+0.2	%/%
DYNAMIC CHARACTERISTICS[6, 8,9]						
Bandwidth −3 dB	BW	Code = 0x80		470		kHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms, V_B = 0 V, f = 1 kHz		0.006		%
V_W Settling Time	t_S	V_A = 10 V, V_B = 0 V, ±1 LSB error band		4		µs
Resistor Noise Voltage	e_{N_WB}	R_{WB} = 5 kΩ, f = 1 kHz		0.9		$nV\sqrt{Hz}$

[1] Typical represent average reading at +25°C, V_{DD} = +15 V, and V_{SS} = −15 V.
[2] Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from an ideal value measured between successive tap positions. Parts are guaranteed monotonic.
[3] All parts have a 35 ppm/°C temperature coefficient.

[4] INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output digital-to-analog converter. $V_A = V_{DD}$ and $V_B = 0$ V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
[5] Resistor Terminals A, B, and W have no limitations on polarity with respect to each other.
[6] Guaranteed by design and not subject to production test.
[7] P_{DISS} is calculated from ($I_{DD} \times V_{DD}$)+abs($I_{SS} \times V_{SS}$). CMOS logic level inputs result in minimum power dissipation.
[8] Bandwidth, noise, and settling times are dependent on the terminal resistance value chosen. The lowest R value results in the fastest settling time and highest bandwidth. The highest R value results in the minimum overall power consumption.
[9] All dynamic characteristics use $V_{DD} = +15$ V and $V_{SS} = -15$ V.

ELECTRICAL CHARACTERISTICS—50 kΩ, 100 kΩ VERSIONS

V_{DD}/V_{SS} = ±15 V ± 10% or ±5 V ± 10%, $V_A = +V_{DD}$, $V_B = V_{SS}$/0 V, −40°C < T_A < +125°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS RHEOSTAT MODE						
Resistor Differential NL[2]	R-DNL	R_{WB}, V_A = NC,	−1	±0.5	+1	LSB
Resistor Nonlinearity[2]	R-INL	R_{WB}, V_A = NC, R_{AB} = 50 kΩ	−1.5	±0.5	+1.5	LSB
		R_{WB}, V_A = NC, R_{AB} = 100 kΩ	−1	±0.5	+1	LSB
Nominal Resistor Tolerance	ΔR_{AB}	T_A = +25°C	−30		+30	%
Resistance Temperature Coefficient[3]	$(\Delta R_{AB}/R_{AB})/\Delta T*10^6$	$V_{AB} = V_{DD}$, wiper = no connect		35		ppm/°C
Wiper Resistance	R_W	V_{DD}/V_{SS} = ±15 V		120	200	Ω
		VDD/VSS = ±5 V		260		Ω
DC CHARACTERISTICS POTENTIOMETER DIVIDER MODE						
Integral Nonlinearity[4]	INL		−1	±0.5	+1	LSB
Differential Nonlinearity[4]	DNL		−1	±0.5	+1	LSB
Voltage Divider Temperature Coefficient	$(\Delta V_W/V_W)/\Delta T*10^6$	Code = 0x80		5		ppm/°C
Full-Scale Error	V_{WFSE}	Code = 0xFF	−2	−0.5	0	LSB
Zero-Scale Error	V_{WZSE}	Code = 0x00	0	+0.5	+1	LSB
RESISTOR TERMINALS						
Voltage Range[5]	$V_{A, B, W}$		V_{SS}		V_{DD}	V
Capacitance[6] A, B	$C_{A, B}$	f = 1 MHz, measured to GND, code = 0x80		45		pF
Capacitance[6]	C_W	f = 1 MHz, measured to GND, code = 0x80		60		pF
Common-Mode Leakage	I_{CM}	$V_A = V_B = V_W$		1		nA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High ($\overline{CS}$, CLK, SDI)	V_{IH}	V_{DD} = 5 V or 15 V	2.4			V
Input Logic Low ($\overline{CS}$, CLK, SDI)	V_{IL}	V_{DD} = 5 V or 15 V			0.8	V
Output Logic High (SDO)	V_{OH}	$R_{Pull-up}$ = 2.2 kΩ to 5 V	4.9			V
Output Logic Low (SDO)	V_{OL}	I_{OL} = 1.6 mA, V_{LOGIC} = 5 V, V_{DD} = 15 V			0.4	V
Input Current	I_{IL}	V_{IN} = 0 V or 5 V			±1	µA
Input Capacitance[6]	C_{IL}			5		pF
POWER SUPPLIES						
Power Supply Range	V_{DD}/V_{SS}	Dual-supply range	±4.5		±16.5	V
Power Supply Range	V_{DD}	Single-supply range, V_{SS} = 0	4.5		33	V
Positive Supply Current	I_{DD}	V_{IH} = +5 V or V_{IL} = 0 V, V_{DD}/V_{SS} = ±15 V			2	mA
		V_{IH} = +5 V or V_{IL} = 0 V, V_{DD}/V_{SS} = ±5 V		12	25	µA
Negative Supply Current	I_{SS}	V_{IH} = +5 V or V_{IL} = 0 V, V_{DD}/V_{SS} = ±15 V			−0.1	mA
		V_{IH} = +5 V or V_{IL} = 0 V, V_{DD}/V_{SS} = ±5 V			−0.1	mA
Power Dissipation[8]	P_{DISS}	V_{IH} = +5 V or V_{IL} = 0 V, V_{DD}/V_{SS} = ±15 V			31.5	mW
Power Supply Rejection Ratio	PSRR		−0.25	±0.1	+0.25	%/%
DYNAMIC CHARACTERISTICS[6, 7, 8]						
Bandwidth −3 dB	BW	R_{AB} = 50 kΩ, code = 0x80		90		kHz
		R_{AB} = 100 kΩ, code = 0x80		50		kHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms, V_B = 0 V, f = 1 kHz		0.002		%
V_W Settling Time	t_S	V_A = 10 V, V_B = 0 V, ±1 LSB error band		4		µs
Resistor Noise Voltage	e_{N_WB}	R_{WB} = 25 kΩ, f = 1 kHz		2		$nV\sqrt{Hz}$

[1] Typical represent average reading at +25°C, VDD = +15 V, and VSS = −15 V.
[2] Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from an ideal value measured between successive tap positions. Parts are guaranteed monotonic.
[3] All parts have a 35 ppm/°C temperature coefficient.
[4] INL and DNL are measured at VW with the RDAC configured as a potentiometer divider similar to a voltage output digital-to-analog converter. VA = VDD and VB = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.

[5] Resistor Terminals A, B, and W have no limitations on polarity with respect to each other.
[6] Guaranteed by design and not subject to production test.
[7] Bandwidth, noise, and settling times are dependent on the terminal resistance value chosen. The lowest R value results in the fastest settling time and highest bandwidth. The highest R value results in the minimum overall power consumption.
[8] All dynamic characteristics use VDD = +15 V and VSS = −15 V.

Table 3.

INTERFACE TIMING CHARACTERISTICS [1]					
Clock Frequency	f_{CLK}			4	MHz
Input Clock Pulse Width	t_{CH}, t_{CL}	Clock level high or low	120		ns
Data Setup Time	t_{DS}		30		ns
Data Hold Time	t_{DH}		20		ns
CLK to SDO Propagation Delay[2]	t_{PD}	$R_{Pull-up}$ = 2.2 kΩ, C_L < 20 pF	10	100	ns
$\overline{CS}$ Setup Time	t_{CSS}		120		ns
$\overline{CS}$ High Pulse Width	t_{CSW}		150		ns
CLK Fall to $\overline{CS}$ Fall Hold Time	t_{CSH0}		10		ns
CLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		120		ns
$\overline{CS}$ Rise to Clock Rise Setup	t_{CS1}		120		ns

[1] See Figure 3 for the location of the measured values. All input control voltages are specified with $t_R = t_F$ = 1 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V. Switching characteristics are measured using V_{DD} = +15 V and V_{SS} = −15 V.
[2] Propagation delay depends on value of V_{DD}, $R_{Pull-up}$, and C_L.

3-WIRE DIGITAL INTERFACE

Table 4. AD5290 Serial Data-Word Format

B7	B6	B5	B4	B3	B2	B1	B0
D7	D6	D5	D4	D3	D2	D1	D0
MSB							LSB
2^7							2^0

NOTE: Data is loaded MSB first.

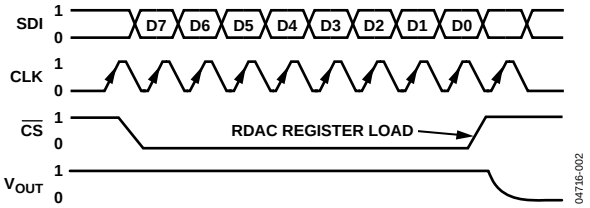


Figure 2. AD5290 3-Wire Digital Interface Timing Diagram ($V_A = V_{DD}$, $V_B = 0$ V, $V_W = V_{OUT}$)

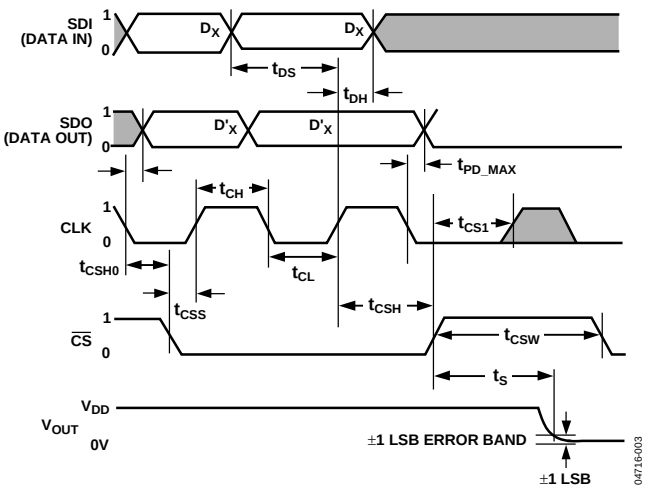


Figure 3. Detail Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = +25°C, unless otherwise noted.

Table 5.

Parameter	Rating
V_{DD} to GND	−0.3 V, +35 V
V_{SS} to GND	+0.3 V, −16.5 V
V_{DD} to V_{SS}	−0.3 V, +35 V
V_A, V_B, V_W to GND	V_{SS}, V_{DD}
Maximum Current	
I_{WB}, I_{WA} Pulsed	±20 mA
I_{WB} Continuous (R_{WB} ≤ 6kΩ, A Open, V_{DD}/V_{SS} = 30V/0V)[1]	±5 mA
I_{WA} Continuous (R_{WA} ≤ 6kΩ, B Open, V_{DD}/V_{SS} = 30V/0V)[1]	±5 mA
Digital Input and Output Voltages to GND	0 V, +7 V
Operating Temperature Range	−40°C to +125°C
Maximum Junction Temperature (T_J MAX)[2]	+150°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 to 30 sec)	245°C
Thermal Resistance[2] θ_{JA}: MSOP-10	230°C/W

[1] Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.

[2] Package power dissipation = $(T_{JMAX} - T_A)/\theta_{JA}$.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND DESCRIPTIONS

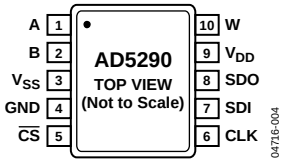


Figure 4. AD5290 Pin Configuration

Table 6. AD5290 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	A	A Terminal. $V_{SS} \le V_A \le V_{DD}$.
2	B	B Terminal. $V_{SS} \le V_B \le V_{DD}$.
3	V_{SS}	Negative Supply. Connect to zero volts for single-supply applications.
4	GND	Digital Ground.
5	$\overline{CS}$	Chip Select Input, Active Low. When $\overline{CS}$ returns high, data is loaded into the wiper register.
6	CLK	Serial Clock Input. Positive edge triggered.
7	SDI	Serial Data Input Pin. Shifts in one bit at a time on positive clock CLK edges. MSB loaded first.
8	SDO	Serial Data Output Pin. Internal N-Ch FET with open-drain output that requires external pull-up resistor. It shifts out the previous 8 SDI bits that allow daisy-chain operation of multiple packages.
9	V_{DD}	Positive Power Supply.
10	W	W Terminal. $V_{SS} \le V_W \le V_{DD}$.

TYPICAL PERFORMANCE CHARACTERISTICS

Figure 5. Resistance Step Position Nonlinearity Error vs. Code

Figure 6. Relative Resistance Step Change from Ideal vs. Code

Figure 7. Potentiometer Divider Nonlinearity Error vs. Code

Figure 8. Potentiometer Divider Differential Nonlinearity Error vs. Code

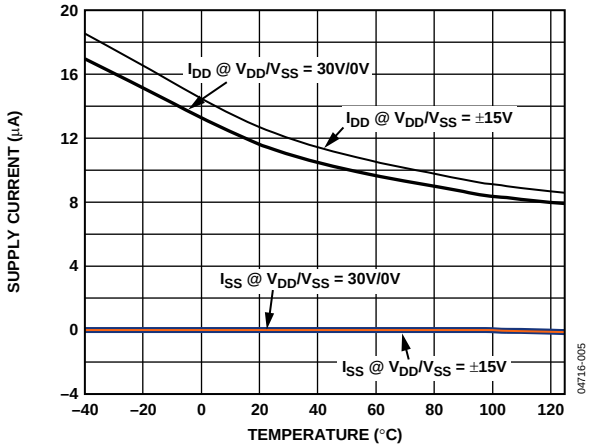


Figure 9. Supply Current (I_{DD}, I_{SS}) vs. Temperature

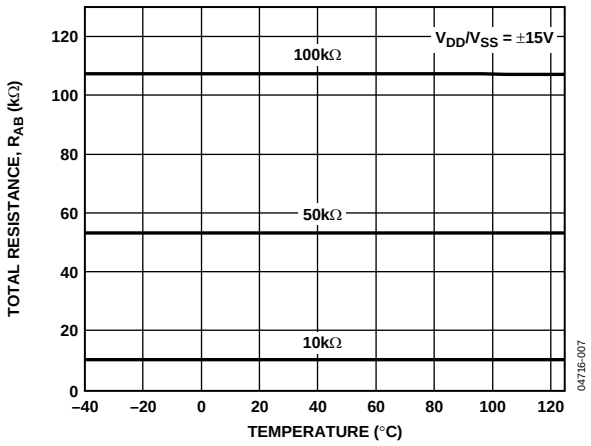


Figure 10. Total Resistance vs. Temperature

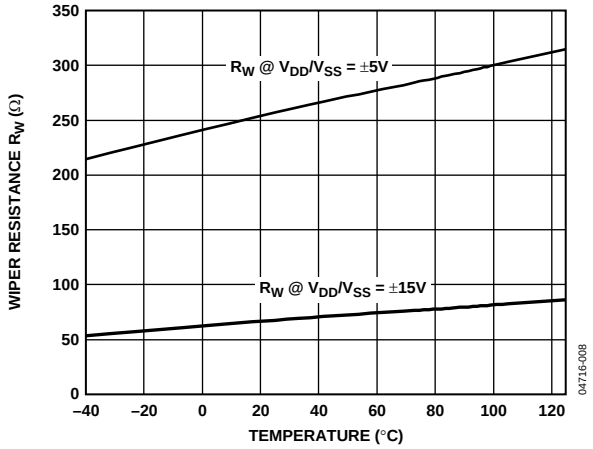


Figure 11. Wiper Contact Resistance vs. Temperature

Figure 12. ($\Delta R_{WB}/R_{WB}$)/ΔT Rheostat Mode Tempco

Figure 13. ($\Delta V_{WB}/V_{WB}$)/ΔT Potentiometer Mode Tempco

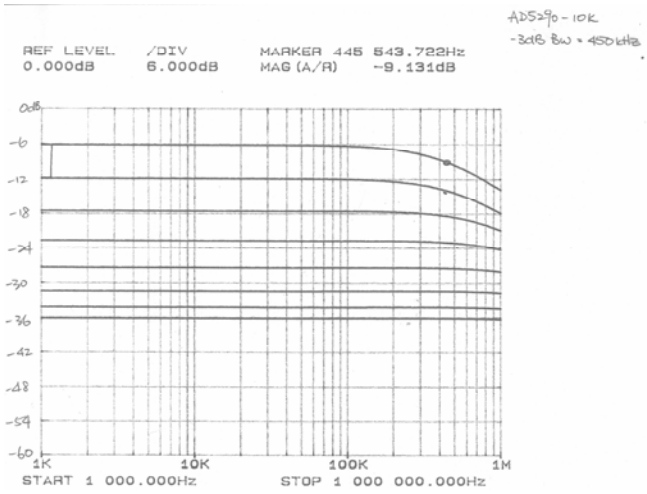


Figure 14. 10 kΩ Gain vs. Frequency vs. Code

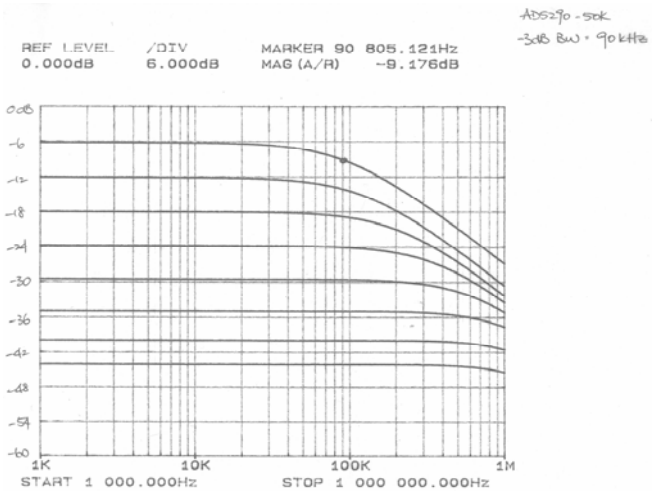


Figure 15. 50 kΩ Gain vs. Frequency vs. Code

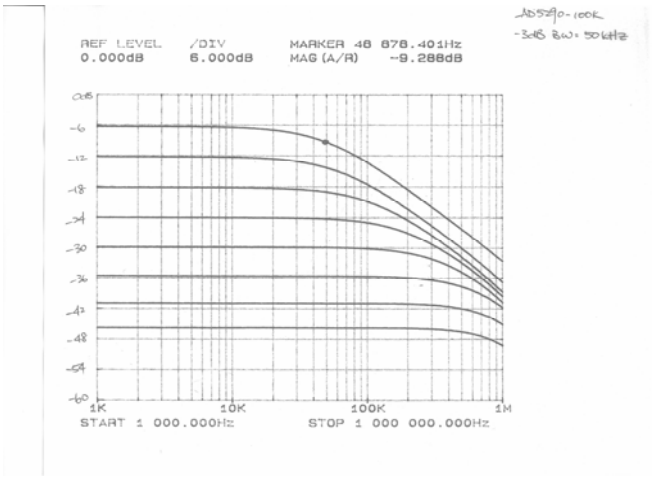


Figure 16. 100 kΩ Gain vs. Frequency vs. Code

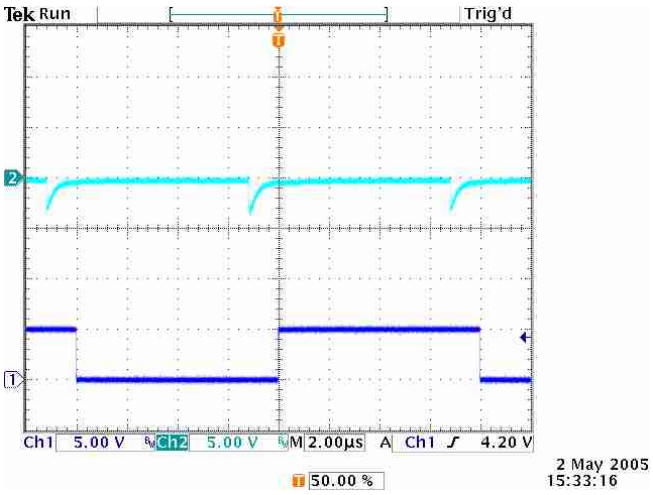


Figure 17. Midscale Transition Glitch

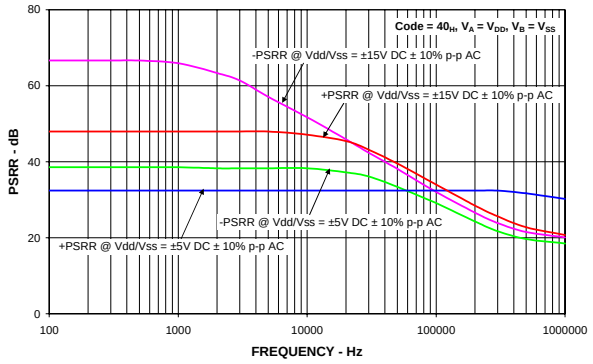


Figure 18. Power Supply Rejection vs. Frequency

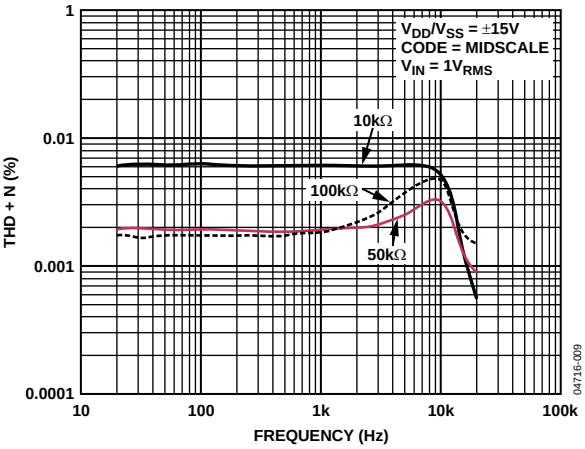


Figure 19. Total Harmonic Distortion Plus Noise vs. Frequency

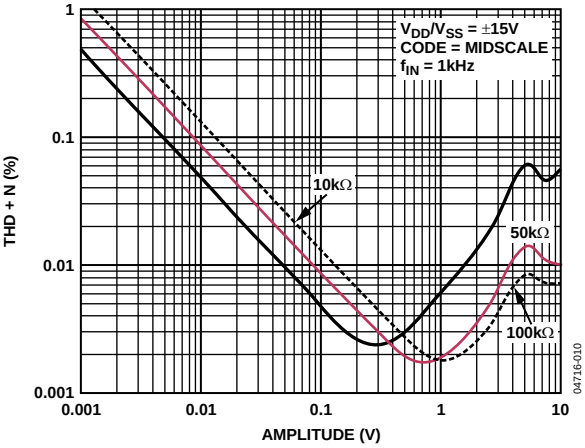


Figure 20. Total Harmonic Distortion Plus Noise vs.Amplitude

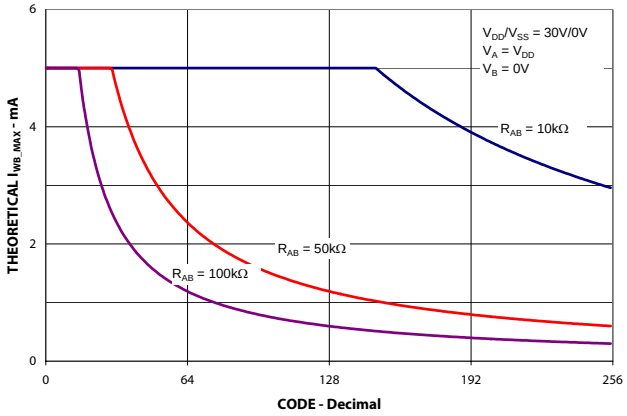


Figure 21. Theoretical Maximum Current vs. Code

THEORY OF OPERATION

PROGRAMMING THE VARIABLE RESISTOR

Rheostat Operation

When only two terminals are used, for example, R_{WA} or R_{WB} as shown in Figure 23, the part operates in rheostat mode. The nominal resistance between terminals A and B, R_{AB} is available in 10 kΩ, 50 kΩ, and 100 kΩ and has 256 tap points accessed by the wiper terminal. The 8-bit data in the RDAC latch is decoded to select one of the 256 possible settings, as shown in Figure 23.

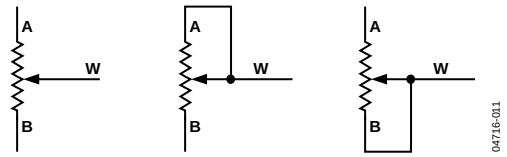


Figure 22. Rheostat Mode Configuration

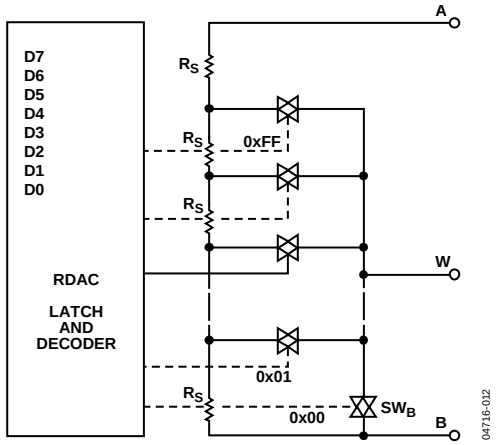


Figure 23. AD5290 Equivalent RDAC Circuit

The general equation determining the digitally programmed output resistance between the W and B terminals is

$$R_{WB}(D) = \frac{D}{256} \times R_{AB} + R_W \qquad (1)$$

where:

D is the decimal equivalent of the binary code loaded in the 8-bit RDAC register from 0 to 256.
R_{AB} is the end-to-end resistance.
R_W is the wiper resistance contributed by the on resistance of the internal switch.

The AD5290 wiper switches are designed with the transmission gate CMOS topology with the gate voltage derived from the V_{DD}. The switch on-resistance, R_W, is not only the function of V_{DD}, but also of temperature; see Figure 11. Additionally, the on resistance for each switch is insensitive to the tap point potential and remains relatively flat as 120 Ω typical at V_{DD} of 15V and the temperature of 25°C.

Assuming that a 10 kΩ part is used, the wiper's first connection starts at the B terminal for programming code of 0x00 where SW_B is closed. The minimum resistance between terminals W and B is, therefore, generally 120 Ω. The second connection is the first tap point, which corresponds to 159 Ω (R_{WB} = 1/256* R_{AB} + R_W = 39 Ω + 120 Ω) for programming code of 0x01, and so on. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at 10,080 Ω (R_{AB} – 1LSB + R_W).

Note that in the zero-scale condition, a finite wiper resistance of 120 Ω is present. Care should be taken to limit the current conducted between the W and B terminals in this state to a maximum pulse current of no more than 20 mA. Otherwise, degradation or possible destruction of the internal switch contact can occur.

Similar to the mechanical potentiometer, the resistance of the RDAC between the W and A terminals also produces a digitally controlled complementary resistance, R_{WA}. When these terminals are used, the B terminal can be opened. Setting the resistance value for R_{WA} starts at a maximum value of resistance and decreases as the data loaded in the latch increases in value. The general equation for this operation is

$$R_{WA}(D) = \frac{256 - D}{256} \times R_{AB} + R_W \qquad (2)$$

Typical device-to-device matching is process-lot dependent and may vary by up to ±30%. Because the resistance element is processed in thin-film technology, the change in R_{AB} with temperature has a very low 35 ppm/°C temperature coefficient.

PROGRAMMING THE POTENTIOMETER DIVIDER

Voltage Output Operation

The digital potentiometer easily generates a voltage divider at wiper-to-B and wiper-to-A proportional to the input voltage at A to B. Unlike the polarity of V_{DD} to GND, which must be positive, voltage across A to B, W to A, and W to B can be at either polarity.

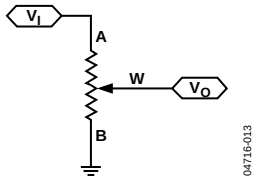


Figure 24. Potentiometer Mode Configuration

If ignoring the effect of the wiper resistance for approximation, connecting the A terminal to 30 V and the B terminal to ground produces an output voltage at the Wiper W to Terminal B ranging from 0 V to 1 LSB less than 30 V. Each LSB of voltage is equal to the voltage applied across terminals A and B, divided by the 256 positions of the potentiometer divider. The general equation defining the output voltage at V_W with respect to ground for any valid input voltage applied to terminals A and B is

$$V_W(D) = \frac{D}{256} V_A \qquad (3)$$

A more accurate calculation, which includes the effect of wiper resistance, V_W, becomes

$$V_W(D) = \frac{R_{WB}(D)}{R_{AB}} V_A + \frac{R_{WA}(D)}{R_{AB}} V_B \qquad (4)$$

Operation of the digital potentiometer in the divider mode results in a more accurate operation over temperature. Unlike the rheostat mode, the output voltage is dependent mainly on the ratio of the internal resistors R_{WA} and R_{WB} and not the absolute values. Therefore, the temperature drift reduces to 5 ppm/°C.

3-WIRE SERIAL BUS DIGITAL INTERFACE

The AD5290 contains a 3-wire digital interface ($\overline{CS}$, CLK, and SDI). The 8-bit serial word must be loaded MSB first. The format of the word is shown in Figure 2. The positive-edge sensitive CLK input requires clean transitions to avoid clocking incorrect data into the serial input register. Standard logic families work well. When $\overline{CS}$ is high, the clock loads data into the serial register on each positive clock edge.

The data setup and data hold times in the specifications tables determine the valid timing requirements. The AD5290 uses an 8-bit serial input data register word that is transferred to the internal RDAC register when the $\overline{CS}$ line returns to logic high. Extra MSB bits are ignored.

DAISY CHAIN OPERATION

SDO shifts out the SDI content in the previous frame; thus it can be used for daisy chain multiple devices. The SDO pin contains an open drain N-Ch MOSFET and requires a pull-up resistor if SDO function is used. Users need to tie the SDO pin of one package to the SDI pin of the next package. Users may need to increase the clock period because the pull-up resistor and the capacitive loading at the SDO-SDI interface may induce time delay to the subsequent devices.

For example, in Figure 25, if two AD5290 are daisy-chained, a total of 16 bits of data are required for each operation. The first set of eight bits goes to U2, and the second set of eight bits goes to U1. The $\overline{CS}$ should be kept low until all 16 bits are clocked into their respective serial registers. The $\overline{CS}$ is then pulled high to complete the operation. When daisy chain multiple devices, users may need to increase the clock period because the pull-up resistor and the capacitive loading at the SDO-SDI interface may induce a time delay to subsequent devices.

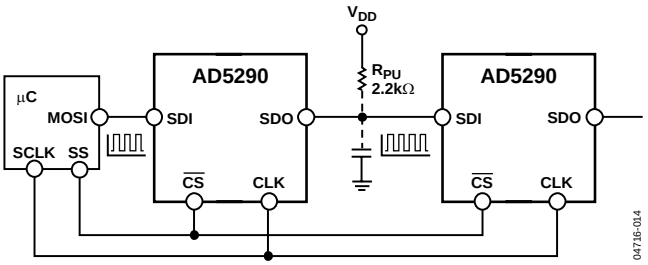


Figure 25. Daisy Chain Configuration

ESD PROTECTION

All digital inputs are protected with a series input resistor and a Zener ESD structure, as shown in Figure 26. These structures apply to digital input pins $\overline{CS}$, CLK, SDI, and SDO.

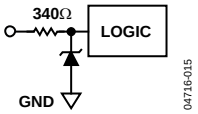


Figure 26. Equivalent ESD Protection Circuit

All analog terminals are also protected by Zener ESD protection diodes, as shown in Figure 27.

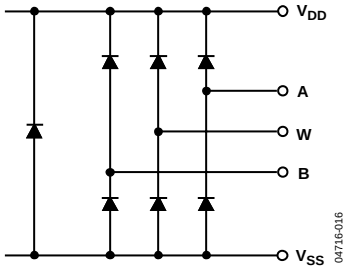


Figure 27. Equivalent ESD Protection Analog Pins

TERMINAL VOLTAGE OPERATING RANGE

The AD5290 V_{DD} and V_{SS} power supplies define the boundary conditions for proper 3-terminal digital potentiometer operation. Applied signals present on Terminals A, B, and W that are more positive than V_{DD} or more negative than V_{SS} are clamped by the internal forward-biased diodes; refer to Figure 27.

POWER-UP AND POWER-DOWN SEQUENCES

Because of the ESD protection diodes that limit the voltage compliance at terminals A, B, and W (refer to Figure 27), it is important to power V_{DD}/V_{SS} before applying any voltage to Terminals A, B, and W. Otherwise, the diodes are forward-biased such that V_{DD}/V_{SS} are powered unintentionally and affect the system. Similarly, V_{DD}/V_{SS} should be powered down last. The ideal power-up sequence is in the following order: GND, V_{DD}, V_{SS}, digital inputs, and $V_A/V_B/V_W$. The order of powering V_A, V_B, V_W, and the digital inputs is not important, as long as they are powered after V_{DD}/V_{SS}.

LAYOUT AND POWER SUPPLY BIASING

It is good practice to use a compact, minimum lead-length layout design. The leads to the input should be as direct as possible, with a minimum conductor length. Ground paths should have low resistance and low inductance.

Similarly, it is also good practice to bypass the power supplies with quality capacitors. Low ESR (equivalent series resistance) 1 µF to 10 µF tantalum or electrolytic capacitors should be applied at the supplies to minimize any transient disturbance and filter low frequency ripple. Figure 28 illustrates the basic supply-bypassing configuration for the AD5290.

The ground pin of the AD5290 is a digital ground reference. To minimize the digital ground bounce, the AD5290 digital ground terminal should be joined remotely to the analog ground; refer to Figure 28.

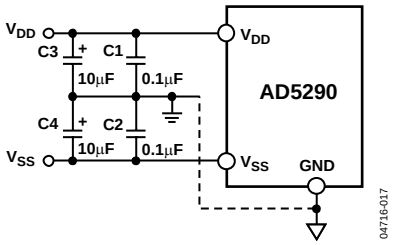


Figure 28. Power Supply Bypassing

APPLICATIONS

High Voltage DAC

AD5290 can be configured as a high voltage DAC, as high as 30 V. The circuit is shown in Figure 29. The output is

$$V_O(D) = \frac{D}{256}[1.2V \times (1 + \frac{R_2}{R_1})] \quad (5)$$

Where *D* is the decimal code from 0 to 255.

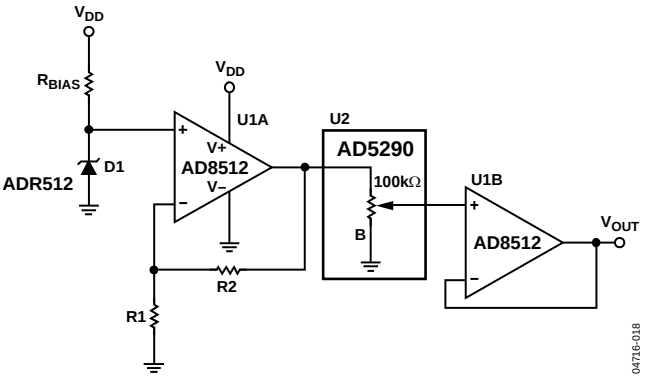


Figure 29. High Voltage DAC

Programmable Power Supply

With a boost regulator, such as ADP1611, AD5290 can be used as the variable resistor at the regulator's FB pin to provide the programmable power supply; see Figure 31. The output is

$$V_O = 1.23V \times (1 + \frac{(D/256) \cdot R_{AB}}{R_2}] \quad (6)$$

Note that AD5290's V_{DD} is derived from the output. Initially, L1 acts as a short, and V_{DD} is one diode voltage drop below +5 V. The output slowly establishes to the final value.

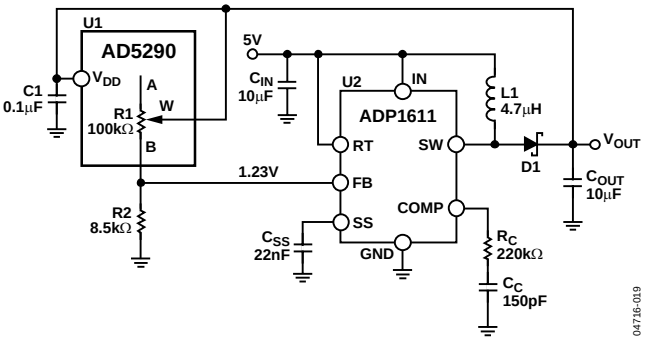


Figure 30. Programmable Power Supply

Audio Volume Control

Because of its good THD performance and high voltage capability, AD5290 can be used as a digital volume control. If AD5290 is used directly as an audio attenuator or gain amplifier, a large step change in the volume level at any arbitrary time can lead to an abrupt discontinuity of the audio signal, causing an audible zipper noise. To prevent this, a zero-crossing window detector can be inserted to the $\overline{CS}$ line to delay the device update until the audio signal crosses the window. Since the input signal can operate on top of any dc levels rather than absolute zero volt level, zero-crossing in this case means the signal is ac coupled and the dc offset level is the signal zero reference point. The configuration to reduce zipper noise and the result of using this configuration are shown in (FIGURE 34 AUDIO VOLUME CONTROL WITH ZIPPER NOISE REDUCTION and FIGURE 35 Input (Trace 1) and Output (Trace 2) of the Circuit), respectively. The input is ac coupled by C1 (Jim, please change C6 to C1) and attenuated down before feeding into the window comparator formed by U_2, U_3, and U_{4B}. U_6 is used to establish the signal zero reference. The upper limit of the comparator is set above its offset and, therefore, the output pulses high whenever the input falls between 2.502 V and 2.497 V (or 0.005 V window) in this example. This output is AND'ed with the chip select signal such that the AD5290 updates whenever the signal crosses the window. To avoid constant update of the device, the chip select signal should be programmed as two pulses, rather than the one shown in FIGURE 2.

In FIGURE 35, the lower trace shows that the volume level changes from a quarter scale to full scale when a signal change occurs near the zero-crossing window.

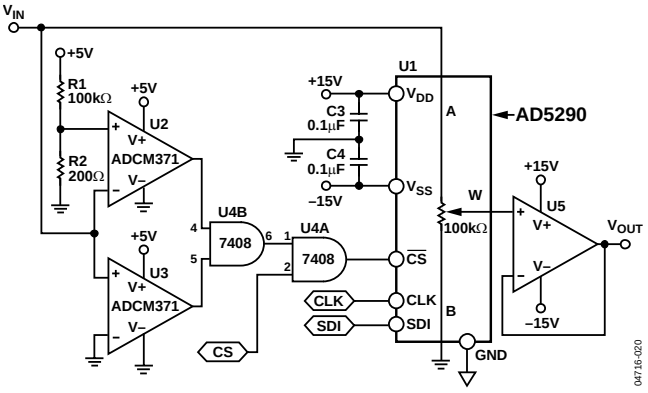
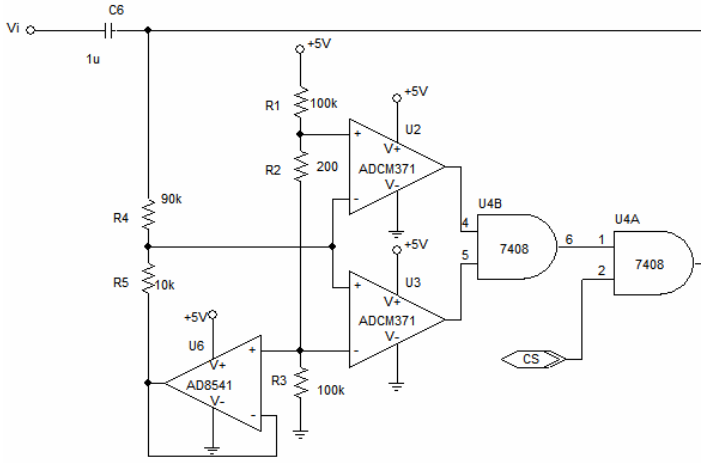


Figure 31. Audio Volume Control with Zipper Noise Reduction



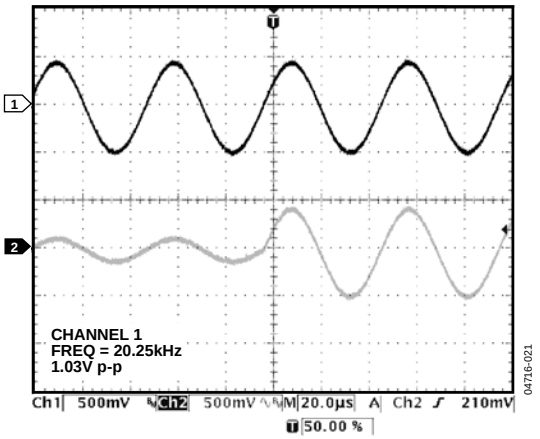


Figure 32. Input and output of the circuit in Figure 32. The lower trace shows that the volume level changes from a quarter scale to full scale with change occurs near zero crossing window.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

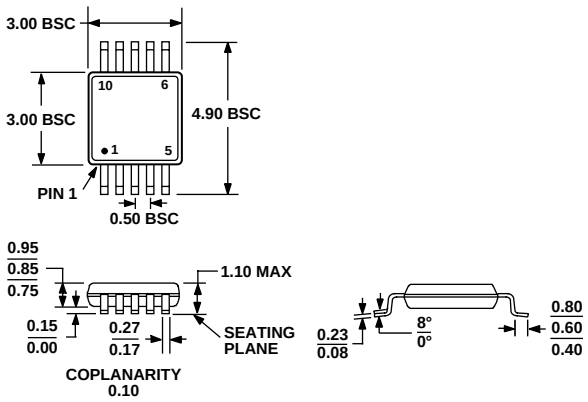


Figure 33. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model	R_{AB} (kΩ)	Temperature Range	Package Description	Package Option	Branding
AD5290YRMZ10[1]	10	–40°C to +125°C	MSOP-10	RM-10	D4U
AD5290YRMZ10-R7[1]	10	–40°C to +125°C	MSOP-10	RM-10	D4U
AD5290YRMZ50[1]	50	–40°C to +125°C	MSOP-10	RM-10	D4T
AD5290YRMZ50-R7[1]	50	–40°C to +125°C	MSOP-10	RM-10	D4T
AD5290YRMZ100[1]	100	–40°C to +125°C	MSOP-10	RM-10	D4V
AD5290YRMZ100-R7[1]	100	–40°C to +125°C	MSOP-10	RM-10	D4V
AD5290EVAL	10		Evaluation Board		

[1] Z = Pb-free part.

NOTES

NOTES

PR04716-0-7/05(PrF)